SYNOPSYS®

DATASHEET

GenSys

RTL Restructuring, Derivative Design and Design Assembly

User friendly solution for RTL assembly, restructuring and modification for new and derivative designs

Overview

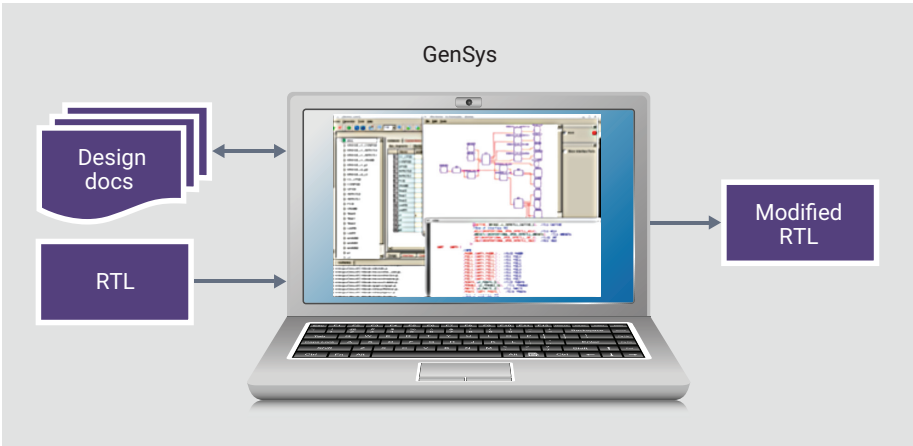
Increased IP reuse in SoC design creates challenges in managing source RTL for systems or subsystem assembly and in handling the RTL modifications needed when creating a new or derivative design. GenSys provides an environment to enable "correct-by-construction" RTL design assembly and includes management and modification tools for RTL restructuring and derivative design that enables improved productivity for front-end designers.

RTL Restructuring and Derivative Design

The process of capturing and managing RTL modifications on a large SoC design can be error-prone, often requiring complex and difficult-to-maintain user scripts. GenSys makes it easy to perform modifications such as hierarchy manipulation, swapping of IP or memory blocks, insertion of new RTL logic at any level of hierarchy and restructuring of existing RTL. It includes schematic and hierarchy views with easy to use drag and drop capabilities, built-in analysis tools, RTL health checks, version tracking and mapping file output for use in formal verification. With an easy-to-use GUI and a Tcl command environment, GenSys speeds up the task of design modification, ensures that no errors are introduced and enables efficient design reuse.

Design Assembly

GenSys provides designers with an environment to perform architectural planning and optimization during chip or sub-design assembly processes. It supports bottom up and top-down methodologies for hierarchical design assembly, allowing users to change the hierarchy on the fly and create or edit components in place. GenSys also includes comprehensive connectivity checking and supports both interface and user-defined connection rules to drive fast completion of many connections.



Key Benefits

- Provides an easy-to-use environment for RTL restructuring and modification for new and derivative designs
- Enables custom logic insertion for DFT/Power at any level of RTL hierarchy
- Enables effective design reuse, automated update of IP/Memories and IP integration
- Enables “correct-by-construction” RTL assembly, reducing the time to create high-quality designs
- Helps dispersed design teams to create more consistent high-quality designs

Key Features

- Supports standard formats, including Verilog, VHDL, System Verilog and Tcl
- Provides batch and graphical use-models that are fully interchangeable
- Supports hierarchy manipulation through GUI/Tcl commands
- Generates setup for logical equivalency checking
- TCL commands to insert logic at any level of RTL hierarchy
- Support automated update of IP/Memories
- Preserves design configurability such as parameter and `define macros
- User-definable auto-connect techniques help complete numerous connections
- Custom report generation through user defined templates